UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
TYLER DIVISION

THE PACID GROUP, LLC, Plaintiff, v. APPLE, INC. et al, Defendants.	Case No. 6:09-CV-143 (LED) (JDL)

DEFENDANTS' MOTION FOR SUMMARY JUDGMENT
OF INDEFINITENESS FOR '646 PATENT CLAIMS 12 AND 26

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I. INTRODUCTION

Plaintiff The PACid Group, LLC ("PACid") alleges that Defendants Atheros Communications, Inc., Broadcom Corporation, Intel Corporation, and Marvell Semiconductor, Inc. (collectively, "Defendants") infringe claims 12 and 26 of U.S. Patent No. 5,963,646 (filed Dec. 28, 1998) ("the '646 patent"). By this motion, Defendants seek summary judgment that these claims are invalid due to indefiniteness, at least because the claims incorporate a means-plus-function limitation unsupported by the '646 patent's specification.

II. STATEMENT OF ISSUES

1. Are claims 12 and 26 of the '646 patent indefinite because the patent lacks sufficient structure corresponding to the means-plus-function limitation "interrupt control means . . . for issuing an interrupt signal upon receipt of said command sequences"?

III. STATEMENT OF UNDISPUTED MATERIAL FACTS

1. PACid has accused each Defendant of infringing claims 12 and 26 of the '646 patent. (Ex. A, PACid Inf. Conts. (Oct. 6, 2009), at 2.)

2. Independent claim 12 reads:

> 12. An encryption key generator in electrical communication with a host system, which comprises:
>
> an I/O interface means in electrical communication with said host system and receiving command sequences from said host system;
>
> interrupt control means in electrical communication with said I/O interface means for issuing an interrupt signal upon receipt of said command sequences;
>
> a ROM in electrical communication with said I/O interface means and having stored therein operating firmware, a bit-shuffle computer program, and a secure hash computer program;
>
> a RAM in electrical communication with said I/O interface means and said ROM for storing a current E-Key Seed and a constant value;
>
> an EEPROM in electrical communication with said I/O interface means, said ROM, and said RAM, for storing said E-Key Seed and said constant value; and
>
> a CPU in electrical communication with said interrupt control, said I/O interface means, said ROM, said RAM, and said EEPROM for executing said bit-shuffle computer program to combine said constant value and said E-Key Seed in a first many-to-few bit mapping, for executing said secure hash algorithm to

> produce a message digest in a second many-to-few bit mapping, and for extracting a pseudo-random symmetric, encryption key from said message digest and storing said encryption key in said EEPROM.

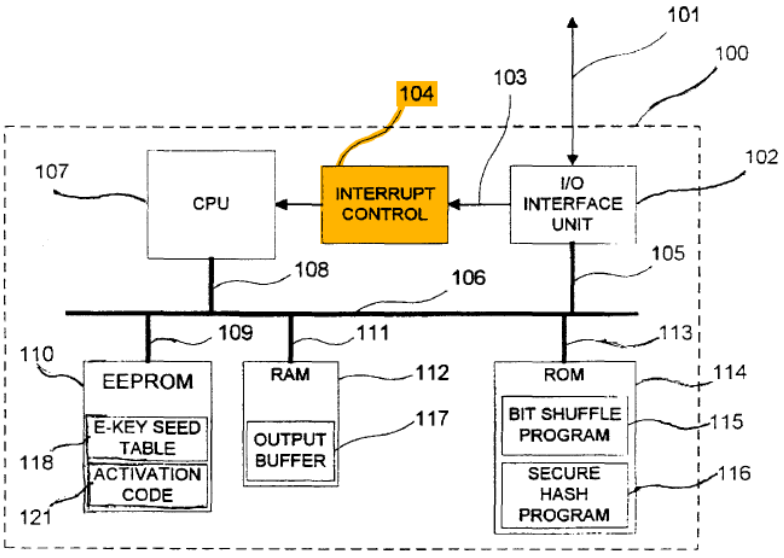
(Ex. B, '646 patent, cl.12 (emphasis added).) Claim 12's "interrupt control means . . . for issuing an interrupt signal upon receipt of said command sequences" limitation is at issue here.

3. Claim 26 requires:

> The system of claim 12, wherein said pseudo-random, symmetric encryption key also is deterministic and non-predictable.

(Id. at cl. 26.) Claim 26 thus includes by reference the "interrupt control means . . . for issuing an interrupt signal upon receipt of said command sequences" requirement of claim 12. No other claim of the '646 patent, asserted or unasserted, references interrupt control.

4. The written description of the '646 patent includes intermittent references to interrupt control. Figure 3 depicts a box labeled "INTERRUPT CONTROL 104."



(Id. at Fig. 3 (highlighting added).) No other figure of the '646 patent depicts element 104 or references interrupt control.

5. The '646 written description includes some discussion of Figure 3 and only passing reference to interrupt control 104:

> Referring to the functional block diagram of FIG. 3, an encryption key generator system 100 is illustrated with a communication bus 101 which is electrically connected to an I/O interface unit 102. Unit 102 in turn is electrically connected by way of a conducting line 103 to an interrupt control unit 104, and by way of a 15 bit bus 105 to an 8 bit address, data and control bus 106.
>
> The Interrupt control unit 104 is electrically connected to an 8 bit, 4.0 MHz CPU 107, which in turn is electrically connected by way of a 23-bit bus 108 to the bus 106. The bus 106 further is electrically connected by way of a 23-bit bus 109 to a non-volatile, 8160 byte, Electrically Erasable Programmable Read Only Memory (EEPROM) 110 in which is stored an E-Key Seed table 118. The bus 106 still further is electrically connected by way of a 23-bit bus 111 to a 246 byte volatile RAM 112, and by way of a 23-bit bus 113 to a 12800 byte ROM 114. Firmware defining the operation of the CPU 107, and including a bit-shuffle program 115 and a secure hash program 116, is stored in the ROM 114.
>
> In operation, a host system (not shown) inputs commands and data to the key generator system 100, and receives status information and processing results from CPU 107 by way of communication bus 101. When information from the host system is written into the I/O interface unit 102, an interrupt is generated by the interrupt control unit 104. In response to the interrupt, the CPU 107 exits from a wait-state and executes a command interpreter program stored in the ROM 114. As a result, the information which has been written into the I/O interface unit 102 is stored in the operating RAM 112.

(Id. at col. 6:43–7:6.)

6. The ’646 patent makes no other mention of interrupt control or to interrupt control/interrupt control unit 104.

7. The ’646 patent suggests that the Figure 3 system could be purchased in a certain Motorola chip:

> In the preferred embodiment described herein, the system of FIG. 3 may be purchased as part number MC68HC05SC28 from Motorola Semiconductor Product Sector Headquarters located at 3102 North 56th Street, Phoenix, Ariz. 85018. The timing parameters and transmission protocols for the system are in accordance with ISO/IEC 7816-3.

(Id. at col. 7:22–29.)

7. For claims 12 and 26, the relevant field is the field of logic design for computer systems, including interfacing with asynchronous interrupt requests. (Ex. C, Mercer Decl., at ¶

10.) A person of ordinary skill in this field at the '646 patent's effective filing date would possess at least a Master's degree in electrical or computer engineering with several years of industrial experience in the design of digital systems and their interface with computer systems. One who possessed extraordinary experience in one of these areas could also be considered to have ordinary skill in the field, even if he did not have the requisite experience in the other area. (Id.)

8. Among those skilled in the art of computer system design, the term "interrupt" refers to a signal that, when received by computer processor running one or more programs, causes the processor or program to suspend its operation temporarily in such a way that the operation can be resumed later. (Id. at ¶ 3.) Interrupts may be communicated by a variety of hardware and software techniques. (Id.)

9. To one of ordinary skill in this field, the terms "interrupt control" and "interrupt control unit" do not refer to a structure. Rather, these terms refer to a function that can be performed in a computer system in numerous different ways. There are multiple design dimensions that are considered by computer designers when they formulate interrupt control structures. One of these dimensions is the format of the signal communicated from the interrupt controller to the processor. (Id. at ¶ 4.)

10. For example, one type of interrupt is the "level-triggered interrupt," in which the interrupt-receiving device is connected to the interrupt-generating device via a physical wire called an interrupt request line. The presence of an interrupt is indicated by the line either having a high-level (binary "1") or low-level (binary "0") voltage. (Id. at ¶ 5.)

11. Another class of interrupts is the "edge-triggered interrupt." (Id. at ¶ 6.) In this technique, the presence of an interrupt is signaled by the transition of voltage on a given line, either from high-level to low-level or vice versa.

12. Implementation of interrupts in a computer system also requires careful consideration of certain timing problems inherent to the interfacing of synchronous and asynchronous logic circuits. (Id. at ¶ 7.) Computer processors have very precise timing requirements; if an interrupt controller sends signals to a processor with inappropriate timing, the controller could have trouble determining whether an interrupt has or has not occurred. (Id.) Thus, one job of an interrupt controller is to reconcile the asynchronous nature of events requiring the processor's attention with the special timing requirements of the processor. (Id. at ¶ 8.) There are myriad possible techniques for solving this problem, but an engineer seeking to select one would need to evaluate each for its compatibility with a given system design and application. (Id.)

13. At least because of the significant variety of techniques available to implement interrupts in computer systems, a skilled artisan reviewing the limitation "interrupt control means in electrical communication with said I/O interface means for issuing an interrupt signal upon receipt of said command sequences" would not understand the '646 patent to disclose a precise structure that performs the function of "issuing an interrupt signal upon receipt of said command sequences" and would be unable to implement the limitation without additional disclosure of the particular interrupt techniques that the drafter actually intended to be used. (Id. at ¶¶ 12–13.)

14. Similarly, a skilled artisan reviewing the specification of the '646 patent would be unable to find sufficient structure in the patent corresponding to the "interrupt control means . . . for issuing an interrupt signal upon receipt of said command sequences" limitation. (Id. at ¶ 13.)

The ’646 patent’s disclosure of interrupt control unit 104 speaks only in terms of the structures to which the unit is connected and not the way the unit works. (Id. at ¶¶ 13–17.) Also, it does not teach that element’s internal design. (Id. at ¶ 14 et seq.) Further, the specification is not even clear as to the number of physical inputs to interrupt control unit 104. (Id. at ¶ 14.)

15. Furthermore, although the ’646 patent mentions that a Motorola “M68HC05SC28” chip may be purchased to practice the entire system of Figure 3, this disclosure does not tell one of ordinary skill in the art the type of interrupt techniques that this chip employed. (Id. at ¶¶ 17–18.) A person of ordinary skill in the art cannot recognize an interrupt control structure by virtue of this part number alone. (Id.) Moreover, extrinsic references discussing this chip do not disclose the chip’s interrupt control techniques such that a person of ordinary skill in the art could know them. (Id. at ¶ 18; see also Exs. C-3–C-5.)

IV. ARGUMENT

A. Summary Judgment Is Appropriate for Issues of Indefiniteness

Summary judgment is appropriate when “the pleadings, depositions, answers to interrogatories, and admissions on file, together with the affidavits, if any, show that there is no genuine issue as to any material fact and that the moving party is entitled to a judgment as a matter of law.” Fed. R. Civ. P. 56; Celotex Corp. v. Catrett, 477 U.S. 317, 322–23 (1986); Ethicon Endo-Surgery, Inc. v. United States Surgical Corp., 149 F.3d 1309, 1315 (Fed. Cir. 1998).

Whether a claim limitation is a means-plus-function limitation is a question of law. Cardiac Pacemakers, Inc. v. St. Jude Med., Inc., 296 F.3d 1106, 1113 (Fed. Cir. 2002). “A determination of indefiniteness is a legal conclusion that is drawn from the court’s performance of its duty as the construer of patent claims [, and] therefore, like claim construction, is a question of law.” Atmel Corp. v. Info. Storage Devices, Inc., 198 F.3d 1374, 1378 (Fed. Cir.

1999); Rpt. and Recs. of Mag. J., Saxon Innovations, LLC v. Nokia Corp., Case No. 6:07-cv-00490-LED-JDL, slip. op. at 4 (E.D. Tex. Jul. 31, 2009) (attached), adopted, 2009 WL 3161403 (E.D. Tex. Sept. 29, 2009). As a question of law, indefiniteness is an issue that is amenable to summary judgment. See, e.g., Net MoneyIN, Inc. v. VeriSign, Inc., 545 F.3d 1359, 1364, 1367 (Fed. Cir. 2008); Saxon, slip. op. at 8; Maurice Mitchell Innovations, L.P. v. Intel Corp., Case No. 2:04-cv-00450-LED, 2006 WL 3447632, *2 (E.D. Tex. Nov. 22, 2006).

B. The "Interrupt Control Means . . . for Issuing an Interrupt Signal . . ." Term Is a Means-Plus-Function Limitation

Independent claims 12 and its dependent claim 26 of the '646 patent include the limitation "interrupt control means in electrical communication with said I/O interface means for issuing an interrupt signal upon receipt of said command sequences." (Ex. B, '646 patent, col. 9:55–57 (emphases added).) The parties dispute whether this "interrupt control means . . . for issuing an interrupt signal" limitation is in means-plus-function format and subject to section 112(6). See 35 U.S.C. § 112, ¶ 6. Because this limitation uses the word "means" in connection with a claimed function (i.e., "issuing an interrupt signal upon receipt of said command sequences"), there is a presumption that this limitation falls within section 112(6). Net MoneyIN, 545 F.3d at 1366 ("A claim element that contains the word 'means' and recites a function is presumed to be drafted in means-plus-function format under 35 U.S.C. § 112.").

A patentee may overcome this presumption only by proving that the claim itself, and not just the specification, recites sufficient structure to perform the claimed function. Id. PACid, however, cannot rebut the presumption here because the claim itself cites no structure beyond the term "interrupt control means" itself. In analogous cases, the Federal Circuit has held that this kind of language merely naming the structure is insufficient to avoid the presumption that section 112(6) applies. In Biomedino, LLC v. Waters Technologies, 490 F.3d 946 (Fed. Cir. 2007), for

example, a patentee could not rebut the presumption of means-plus-function treatment for the claim limitation "control means for automatically operating [a valve]" merely by pointing to the word "control" as providing structure. 490 F.3d at 950. Similarly, in Callicrate v. Wadsworth Manufacturing, Inc., 427 F.3d 1361 (Fed. Cir. 2005), the patentee could not overcome the presumption that the claim term "cutting means for cutting elastomeric ligature material" warranted means-plus-function treatment based on the claims use of the adjective "cutting" before "means." 427 F.3d at 1369; see also Signtech USA, Ltd. v. Vutek, Inc., 174 F.3d 1352, 1356 (Fed. Cir. 1999) (holding that no structure appears in the limitation "ink delivery means").

Like the limitations in the cases cited above, the "interrupt control means . . . for issuing an interrupt signal" limitation does not disclose sufficient structure to overcome the presumption that section 112(6) applies. Indeed, this limitation recites no structure for performing the function of "issuing an interrupt signal." (Ex. C, Mercer Decl., at ¶ 12.) This failure to recite structure is critical because, as discussed above, in the field of computer system design, interrupts can be generated using a variety of formats—e.g., level-triggered interrupts, edge-triggered interrupts—and with a variety of solutions to inherent timing problems, but the "interrupt control means" limitation speaks to none of these particular structures. (See id. at ¶¶ 5–8, 12.) Moreover, the term "interrupt control" itself is not a well-known structure such that its inclusion before the word "means" is sufficient to rebut the presumption. (See id. at ¶ 4.)

The limitation's statement that the claimed "interrupt control means" will be "in electrical communication with said I/O interface means" gives only high-level guidance as to the positioning of the "interrupt control means" within the claimed system. This language does not teach a skilled artisan about the structure of the interrupt system itself or the way the interrupt system will be implemented. (Id. at ¶ 12.) Similarly, the statement that the claimed means will

"issu[e] an interrupt signal upon receipt of said command sequences" does not teach a structure to be used in generating or handling the interrupt. (Id.)

Both of PACid's arguments that section 112(6) does not apply fail on the merits. First, PACid argues that the term "interrupt control" connotes a well-known structure in the art (PACid Claim Constr. Br., Feb. 19, 2010 (Dkt. #251) at 11), but its source provides a definition for only the term "interrupt." (Id. Ex. C at 583.) By conspicuously failing to provide a definition for the term "interrupt control," PACid's own evidence shows that "interrupt control" does not connote a well-known structure. Thus, the modifier "interrupt control" before "means" in the "interrupt control means . . . for issuing an interrupt signal" limitation cannot rebut the presumption that section 112(6) applies.

Second, PACid argues that that an "interrupt control unit defines a structure to one of ordinary skill in the art."[1] (Id. (emphasis added).) The claim, however, does not recite an "interrupt control unit." Again, to rebut the presumption, the claim itself must recite structure that performs the claimed function. Net MoneyIN, 545 F.3d at 1366. Therefore, PACid's argument that "interrupt control unit" connotes a specific structure is irrelevant to rebutting the presumption.

Because PACid cannot rebut the presumption that the limitation is in means-plus-function form, this Court should analyze the limitation under section 112(6).

C. A Patentee Who Uses a Means-Plus-Function Limitation Has a Duty To Disclose and Link Structure Sufficient To Practice That Limitation

"Section 112, ¶ 6, as is well-documented, was intended to permit use of means expressions without recitation of all the possible means that might be used in a claimed

[1] As discussed infra, "interrupt control unit" is not a well-known structure to one of ordinary skill in the art. PACid's own evidence demonstrates this point because the dictionary cited does not provide a definition for "interrupt control unit." (See PACid Claim Constr. Br., Feb. 19, 2010 (Dkt. #251), Ex. C, at 583.)

apparatus. The price that must be paid for use of that convenience is limitation of the claim to the means specified in the written description and equivalence thereof." O.I. Corp. v. Tekmar Co., 115 F.3d 1576, 1583 (Fed. Cir. 1997); see also 35 U.S.C. § 112, ¶ 6.[2] "If the specification is not clear as to the structure that the patentee intends to correspond to the claimed function, then the patentee has not paid that price but rather is attempting to claim in functional terms unbounded by any reference to structure in the specification[,] [which] . . . is impermissible under the statute." Med. Instrumentation and Diagnostics Corp. v. Elekta AB, 344 F.3d 1205, 1211 (Fed. Cir. 2003); see also Saxon, slip. op. at 5 (quoting Default Proof Credit Sys., Inc. v. Home Depot U.S.A., Inc., 412 F.3d 1291, 1298 (Fed. Cir. 2005) ("This duty to link or associate structure to function is the quid pro quo of employing § 112, ¶ 6.")); Maurice Mitchell, 2006 WL 3447632 at *2.

If the specification lacks disclosure of the structure that performs the recited means or fails to link disclosed structure to the means, the claim is indefinite and, therefore, invalid:

> Although paragraph six statutorily provides that one may use means-plus-function language in a claim, one is still subject to the requirement that a claim "particularly point out and distinctly claim" the invention. Therefore, if one employs means-plus-function language in a claim, one must set forth in the specification an adequate disclosure showing what is meant by that language. If an applicant fails to set forth an adequate disclosure, the applicant has in effect failed to particularly point out and distinctly claim the invention as required by the second paragraph of section 112.

In re Donaldson Co., 16 F.3d 1189, 1195 (Fed. Cir. 1995) (en banc); see also 35 U.S.C. § 112, ¶ 2. To determine whether a patentee disclosed sufficient structure to support a means-plus-

[2] Section 112(6) provides:

> An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

35 U.S.C. § 112, ¶ 6 (emphasis added).

function limitation, one analyzes the limitation and specification from the perspective of one skilled in the art. Atmel, 198 F.3d at 1379–80. "In order for a means-plus-function element to be valid under §112, the corresponding structure of the limitation 'must be disclosed in the written description in such a manner that one skilled in the art will know and understand what structure corresponds to the means limitation.'" Biomedino, 490 F.3d at 950 (quoting Atmel, 198 F.3d at 1381).

Application of the skilled artisan's perspective does not, however, relieve a patentee of his duty to disclose and link structure sufficient to show "what is meant by the claim language." Atmel, 198 F.3d at 1380. The skilled artisan must be able to identify disclosure in the specification of supporting structure:

> It is not enough for the patentee simply to state or later argue that persons of ordinary skill in the art would know what structures to use to accomplish the claimed function. . . . "The inquiry is whether one of skill in the art would understand the specification itself to disclose a structure, not simply whether that person would be capable of implementing that structure."

Aristocrat Techs. Australia Pty Ltd. v. Int'l Game Tech., 521 F.3d 1328, 1336–37 (Fed. Cir. 2008) (quoting Biomedino, 490 F.3d at 953) (emphasis added). Significantly, "the specification itself" must disclose structure that performs the claimed function without resort to external sources. Atmel, 198 F.3d at 1382 (holding that one may not resort to documents incorporated by reference into the patent to identify corresponding structure but must find such structure in the specification). As the Atmel court noted, section 112(2)'s requirements are closely related to both enablement and best mode—in all cases, the Patent Act applies robust disclosure requirements in order to prove that the inventor possesses his invention at the time of filing (enablement), educate the public completely (best mode), and ensure clear and understandable claims (definiteness). Id. at 1379–80.

Each of the above cases shows that unsupported means-plus-function limitations lead to invalid claims under section 112(2). Cases reaching the opposite result—i.e., cases where means-plus-function limitations met section 112(2)'s definiteness requirement—illuminate the same test from the other direction. For example, in Intel Corp. v. Via Technologies, Inc., 319 F.3d 1357 (Fed. Cir. 2003), means-plus-function limitations were sufficiently definite where the specification described in detail the technology that would be used to implement the limitation. 319 F.3d at 1366. Similarly, in S3 Inc. v. NVIDIA Corp., 259 F.3d 1364 (Fed. Cir. 2001), a means-plus-function limitation met section 112(2)'s test where the uncontroverted evidence showed that the specification's disclosure fully informed a skilled artisan about precisely how to implement the limitation—the artisan could implement it "readily" and without uncertainty as to the techniques used. 259 F.3d at 1371.

D. The '646 Patent Fails To Disclose or Link Sufficient Structure Corresponding to the "Interrupt Control Means . . . for Issuing an Interrupt Signal . . ." Term

The '646 patent's specification does not disclose a structure for implementing the claimed "interrupt control means . . . for issuing an interrupt signal upon receipt of said command sequences." Instead, the '646 patent's specification merely refers to the location of the means within the system and assumes that the reader will design some particular interrupt control structure on his own. Because this disclosure is insufficient under section 112(2), claims 12 and 26, which contain the "interrupt control means . . . for issuing an interrupt signal . . ." limitation, are invalid.

1. Disclosure of Interrupt Control 104 Fails to Provide the Required Structure

Figure 3 shows "INTERRUPT CONTROL 104" as a box connected via arrows to "I/O INTERFACE UNIT 102" and "CPU 107." This depiction suggests where the claimed interrupt

control means may be located but not its structure or the way it operates. (See Ex. B, '646 patent, Fig. 3.) A skilled artisan could not implement interrupt control based on this disclosure because it lacks any discussion of the structure or operation of "INTERRUPT CONTROL 104," or even the number of physical inputs to that element. (Ex. C, Mercer Decl., at ¶ 14.)

The patent's written discussion of "interrupt control unit 104" is no more helpful. To one of ordinary skill in the relevant art, the terms "interrupt control" and "interrupt control unit" do not refer to a well-known structure. (Id. at ¶ 4.) Therefore, the written description must describe technical details about the structure and operation of this element in order for one of ordinary skill in the art to know the precise structure to which this "interrupt control unit" refers. As with Figure 3, the text stating that this unit is "electrically connected by way of a conducting line 103" to I/O interface unit 102 fails to describe the structure or operation of the unit. (See Ex. B, '646 patent, col. 6:46–48; Ex. C, Mercer Decl., at ¶¶ 15–16.)

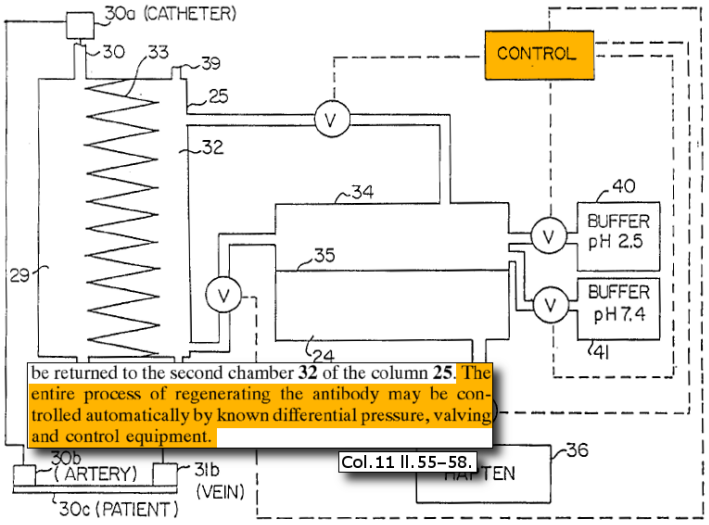
The same is true of the disclosure that interrupt control unit 104 "is electrically connected to an 8 bit, 4.0 MHz CPU 107, which in turn is electrically connected by way of a 23-bit bus 108 to the bus 106." (See Ex. B, '646 patent, col. 6:50–52.) This second passage teaches the structure to which the interrupt control means would be connected, but the passage does not teach the skilled artisan, for example, whether the claimed interrupt means uses level or edge-triggered interrupts, anything about the way to solve the difficult timing problems inherent when bridging synchronous and asynchronous logic, or anything about the structure of the interrupt control means. (Ex. C, Mercer Decl., at ¶¶ 14–15.)

The '646 patent's final discussion of the interrupt control unit 104 is no more instructive:

> When information from the host system is written into the I/O interface unit 102, an interrupt is generated by the interrupt control unit 104. In response to the interrupt, the CPU 107 exits from a wait-state and executes a command interpreter program stored in the ROM 114.

(Ex. B, '646 patent, col. 6:66–7:6.) This disclosure merely repeats the definition of an interrupt—a signal that causes a program or processor to suspend its operations in such a way that they can be resumed later.[3] Because this disclosure says nothing about the structure or technique used to accomplish this end, a skilled artisan reading the patent is left to implement his own interrupt control system without the benefit of instruction from the patentee about the structure that performs the function of issuing an interrupt signal upon receipt of said command sequences in the '646 patent. (See Ex. C, Mercer Decl., at ¶ 16.)

The '646 patent's disclosure of the black box "interrupt control 104" is even less teaching than the disclosure that the Biomedino court held insufficient. In Biomedino, the written description taught only a "black box" for the means-plus-function limitation "control means," and the Federal Circuit invalidated the claim under section 112(2). 490 F.3d at 950–52. Notably, the patent in Biomedino included a figure with a box labeled "CONTROL" and a disclosure that control could be by "known differential pressure, valving, and control equipment":



[3] Here, the program being suspended is apparently a "wait-state" for the processor.

(Ex. D, U.S. Patent No. 6,602,502 (filed May 13, 1991), Fig. 6 and col. 11:55–58 (highlighting and annotation added).)

The Biomedino court rejected the patentee's argument that this disclosure was sufficient structure to support a means-plus-function limitation, explaining that "a bare statement that known techniques or methods can be used does not disclose structure." Biomedino, 490 F.3d at 953 (emphasis added). Although a person of ordinary skill reading the patent in Biomedino might have been able to design a control system on his own, the Biomedino specification was insufficient to teach that person anything about the control system actually being used in the preferred embodiment. Id.

Here, the '646 patent's black box for the interrupt control 104 does not even instruct one of ordinary skill in the art that known techniques of issuing interrupt signals could be used. (Ex. C, Mercer Decl., at ¶ 14.) Instead, the patent invites one of ordinary skill in the art to design his own interrupt control mechanism. (Id. at ¶ 14.) Furthermore, because the '646 patent does not provide even the slightest guidance about the format of the signal communicated from the interrupt controller to the processor or how to solve certain timing problems inherent to the interfacing of synchronous and asynchronous logic circuits (id. at ¶¶ 12–16), the patent fails to provide the kind of disclosure that would allow one of ordinary skill in the art to implement the interrupt control function. See Via Techs., 319 F.3d at 1365 (finding a limitation definite where specification disclosed a detailed approach to performing the recited function); see also Atmel, 198 F.3d at 1382; Biomedino, 490 F.3d at 950.

Therefore, the '646 patent does not comply with section 112(2), and claims 12 and 26 are invalid. See Saxon, slip op. at 7–8 (holding a 112(6) claim indefinite where, inter alia, the patentee contended that the corresponding structure was logic internal to the CPU, but the patent

did not disclose any logic internal to the CPU for performing the recited function or otherwise); Maurice Mitchell, 2006 WL 3447632, *4 (holding 112(6) claim indefinite, inter alia, where the patent disclosed a "plurality of logical elements," which the patentee argued one of ordinary skill in the art would understand meant tri-state circuitry, but did not mention tri-state circuitry itself).

2. Disclosure of the Motorola MC65HC05SC28 Chip Fails To Provide the Required Structure

The '646 patent's statement that the system of Figure 3 could be implemented in a Motorola MC65HC05SC28 chip cannot save these means-plus-function claims for two reasons. (See Ex. B, '646 patent, col. 7:22–25.) First, the '646 patent discloses that the Motorola chip implements the entire system, not the "interrupt control means . . . for issuing an interrupt signal upon receipt of said command sequences." Nothing in the '646 patent teaches how, if at all, the Motorola chip implemented interrupt control. Second, the Motorola chip part number does not tell one of ordinary skill in the art the techniques used for interrupt control in that chip. (Ex. C, Mercer Decl., at ¶¶ 17–18.) As a result, the '646 patent's disclosure of the part number of the Motorola chip would not tell a skilled artisan how to implement the claimed "interrupt control means . . . for issuing an interrupt signal . . . ." (Id.)

Moreover, PACid cannot look to the Motorola chip itself to provide the missing structure. Indeed, Atmel mandates that the disclosure reside in the specification itself and precludes reliance on extrinsic evidence to substantiate the structure. Atmel, 198 F.3d at 1382. Thus, any attempt to remedy the '646 patent's disclosure with reference to the Motorola MC65HC05SC28 chip is unavailing.

To be sure, even if extrinsic evidence is examined, it establishes that Motorola did not publicly disclose the interrupt control structure of the Motorola MC65HC05SC28 chip. (Ex. C, Mercer Decl., at ¶¶ 17–18; see also Exs. C-3–C-5 (extrinsic evidence concerning Motorola

chip).) These extrinsic documents merely discuss the Motorola chip's high-level capabilities and architecture. (See id.) They do not go into any meaningful detail about, for example, whether that chip used edge-triggered interrupts or level-triggered interrupts. (Id.) These specifications also do not disclose the way that the Motorola chip synchronizes interrupts with the CPU clock. (Id.) Therefore, the Motorola specifications further support the conclusion that reference to this part number alone does not teach one of ordinary skill in the art any precise structure or way to implement the claimed "interrupt control means . . . for issuing an interrupt signal upon receipt of said command sequences."

V. CONCLUSION

PACid simply has not paid the price necessary to avail itself of the convenience offered by the means-plus-function format. Because the '646 patent does not disclose any structure that performs the function of "issuing an interrupt signal upon receipt of said command sequences," the "interrupt control means . . . for issuing an interrupt signal upon receipt of said command sequences" limitation is indefinite. Therefore, claims 12 and 26, which include that limitation, are invalid under 35 U.S.C. § 112, ¶ 2, and this Court should enter summary judgment of invalidity for those claims.

Dated: March 5, 2010

Respectfully submitted,

/s/ Jonah D. Mitchell (with permission)

Scott D. Baker (admitted pro hac vice)
John P. Bovich (admitted pro hac vice)
Jonah D. Mitchell (admitted pro hac vice)
James A. Daire (admitted pro hac vice)
REED SMITH LLP
Two Embarcadero Center, Suite 2000
San Francisco, CA 94111-3922
Telephone: (415) 543-8700
Facsimile: (415) 391-8269
Email: sbaker@reedsmith.com
Email: jmitchell@reedsmith.com

Rickey L. Faulkner
State Bar No. 06857095
LAW OFFICE OF RICKEY L. FAULKNER, PC
P.O. Box 3367
Longview, TX 75606
Telephone: (903) 248-8246
Facsimile: (903) 248-8249
Email: rick@faulknerlawoffice.com

Counsel for ATHEROS COMMUNICATIONS, INC.

/s/ Yar R. Chaikovsky (with permission)

Yar R. Chaikovsky
John Lee
MCDERMOTT WILL & EMERY LLP
275 Middlefield Road, Suite 100
Menlo Park, California 94025
Telephone: (650) 815-7400
Facsimile: (650) 815-7401
Email: ychaikovsky@mwe.com

Counsel for BROADCOM CORPORATION

/s/ Lauren A. Degnan
Ruffin B. Cordell
State Bar No. 04820550
Lauren Degnan (admitted pro hac vice)
Rob Courtney (admitted pro hac vice)
FISH & RICHARDSON P.C.
1425 K Street NW, 11th Floor
Washington, DC 20005
Telephone: (202) 783-5070
Facsimile: (202) 783-2331
Email: rbc@fr.com
Email: lad@fr.com

Michael E. Jones
State Bar No. 10929400
POTTER MINTON
A Professional Corporation
110 N. College, Suite 500 (75702)
P.O. Box 359
Tyler, TX 75710
Telephone: (903) 597-8311
Facsimile: (903) 593-0846
Email: mikejones@potterminton.com

Counsel for INTEL CORPORATION

/s/ Brian Range (with permission)
James C. Yoon (admitted pro hac vice)
Ron E. Shulman (admitted pro hac vice)
Brian Range
State Bar No. 24033106
WILSON SONSINI GOODRICH & ROSATI, Professional Corporation
650 Page Mill Road
Palo Alto, California 94304-1050
Telephone: (650) 493-9300
Facsimile: (650) 565-5100
Email: jyoon@wsgr.com
Email: rshulman@wsgr.com
Email: brange@wsgr.com

Andy Tindel
State Bar No. 20054500
PROVOST UMPHREY LAW FIRM, L.L.P.
112 East Line Street, Suite 304
Tyler, Texas 75702
Telephone: (903) 596-0900
Facsimile: (903) 596-0909
Email: atindel@andytindel.com

Counsel for MARVELL SEMICONDUCTOR INC.

CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM-ECF System per Local Rule CV-5(a)(3) on this 5th day of March, 2010. Any other counsel of record will be served by first class mail on this same date.

/s/ Lauren A. Degnan
Lauren A. Degnan
FISH & RICHARDSON P.C.